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Performance Comparision and Design of different CSLA Archtecture using FPGA

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Abstract

Carry select adder (CSLA) is the faster adder used in many computational systems to alleviate the problem of carry propagation delay. It consists of two ripple carry adders (RCA) and multiplexer (mux). To reduce the power in the CSLA an efficient gate level modification is used. The comparison of results analysis shows that the modified SQRT CSLA structure has better performance than the regular SQRT CSLA. Carry select adder using BEC-1 converter is very much efficient in VLSI implementation is designed here.

Keywords: Field programmable logic device (FPGA), CSLA.

Introduction

The need for low-power VLSI system arises from, the steady growth of operating frequency and processing capacity per chip. The heat due to large power consumption must be removed by proper cooling techniques. Battery life in portable devices is limited. For prolonged operation time in the portable devices, Low power design is used as a result of which the speed and area of the CSLA is a major design issue [1].

Area, power and delay are, three most widely parameters used for measuring the circuit. Reducing power consumption has become primary design goal [2].

Carry select adder (CSLA) is the fastest adder used in data processing. It performs arithmetic function. CSLA consists of two ripple carry adder (RCA), Adding two n-bit number with a carry select adder is done with two ripple carry adders in order to perform calculation twice one time with the assumption of carry being zero and other assuming carry one, the final sum and carry are selected by the multiplexer (mux) [3]. It uses multiple pair of ripple carry adder (RCA)[4]

The modified CSLA using BEC consist of AND, OR and NOT gate has reduced power [5].

IIBEC

Binary to excess converter instead of the ripple carry adder is used in this work, n+1 bit BEC is used to replace n-bit RCA. Binary to excess-1 converter in the regular CSLA is used to achieve increase in the operation speed. 2 ripple carry one for cin=0,cin=1in regular CSLA, cin=1 RCA is replaced by BEC. The basic function of the CSLA is obtained by using a 6-bit BEC is shown in figure. The Boolean expression of the 6-bit BEC is

X0= ~B0

X1=B0^B1

X2=B2^(BO&B1)

X3=B3^(B0&B1&B2)

X4=B4^(B0&B1&B2&B3)

X5=B5^(B0&B1&B2&B3&B4)

Table 1:-Function table of 6-bit BEC

B[5:0]	X[5:0]
000000	000001
000001	00010
111111	000000

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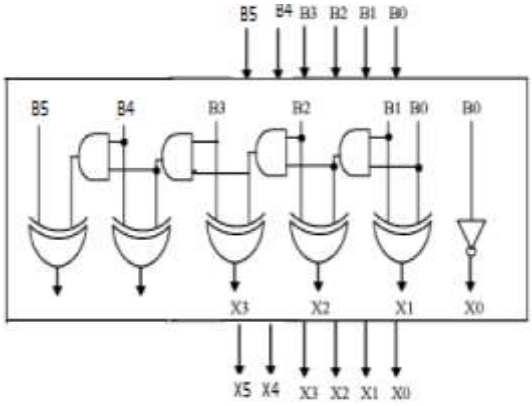

Figure 1 16-Bit BEC without mux

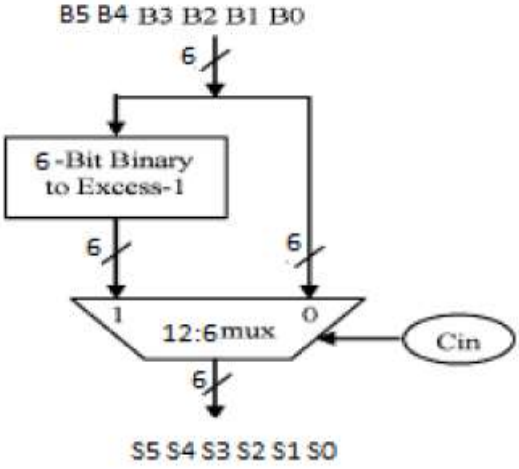

Fig 2:-6-Bit BEC with 6:1 mux

Modified CSLA

Modified CSLA have architecture is similar to regular CSLA, the only change is that, in this binary to excess-1 converter (BEC) is used instead of RCA with cin=1 to achieve low power and reducing n bit RCA with n+1 bit BEC.

Regular CSLA

The architecture of regular CSLA is shown in fig 2 consist of RCA is simple, which allow fast design time, however RCA is relatively slow [6]. Two RCA cin=0 and cin=1 used and final sum and carry are selected by mux For cin=0 half adder is used and for full adder cin=1 used, it is divided into 5-groups.

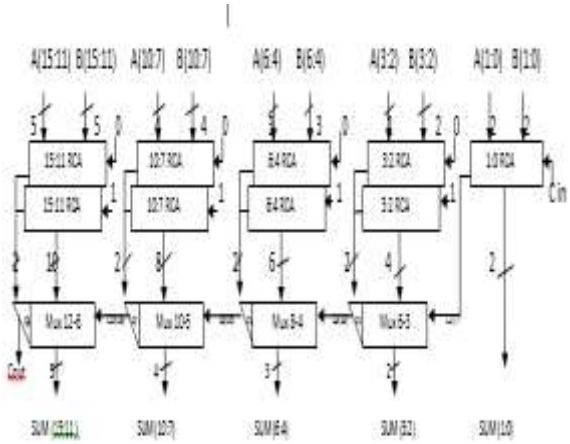

Figure 3 Architecture of regular CSLA

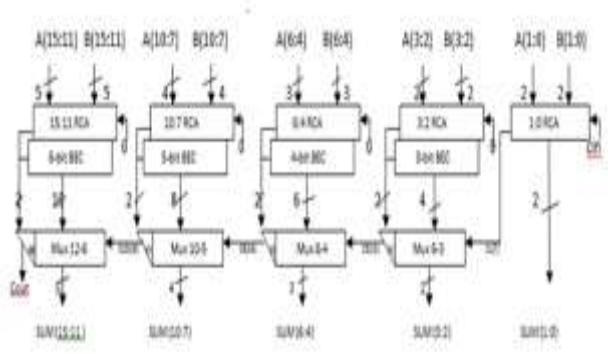

Figure 4 Architecture of modified CSLA

The modified SQRT CSLA is also divided into various groups having the RCA, BEC and mux. XOR gate is used in modified CSLA to optimise and it verifys that large reduction in no. of gates.

The advantage of this BEC logic comes from lesser number of logic gates. It has 5 groups of different size RCA.The design code for the BEC was designed by using NOT, AND and XOR gates.

Results

Power consumptionss

Calculation of Estimate power consumption is very complex

Power consumption is design dependent effected by:-

a) Output loading for the design
b) Performance of System
c) Density of Design and Design activity
d) Logic blocks and interconnect
e) Supply voltage for the design

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Power calculations can be performed at three distinct phase of the design cycle

- **Concept phase**:- In concept phase power estimation is based on logic capability estimation and activity rate, using Xilinx power estimate spread sheed.
- **Design phase**:- more accurate power is calculated based on detailed information about the design implemention in the FPGA, using X-power analyser.
- **System integration phase**:- In this phase power is calculated in a lab environment, using actual instrument. Accurate power calculation at an early stage in the design cycle results in fewer problems.

The design proposed in this paper has been developed using Hardware design language-HDL and synthesized in Xilinx ISE tool. The same value changed dump (VCD) file is generated for all possible input conditions for each word size of the adder and imported the same to Xilinx ISE Power Analysis to perform the power simulations, for both the regular and modified SQRT CSLA. The synthesized report contains power values for adders.

Table 2:-Power report of regular CSLA

Power Supply Summary			
	Total	Dynamic	Static Power
Supply Power (mW)	30.35	16.50	13.85

Table 3:-Power report of modified CSLA

Power Supply Summary			
	Total	Dynamic	Static Power
Supply Power (mW)	25.16	11.36	13.79

Table 4 : Comparision of Modified and Regular structure power

Supply power (mW)		
	Modified CSLA	Regular CSLA
Static Power	13.79	13.85
Dynamic	11.36	16.50
Total	25.16	30.35

Conclusion

A simple approach is proposed in this paper to reduce the power of SQRT CSLA and design regular and modified CSLA. The comaparision of results shows that the modified SQRT CSLA has less power consumtion than the regular design. The reduction in number of gates is obtained by simply replacing the RCA with BEC in the structure. The modified CSLA architechure is therefore low power, simple and efficient for VLSI hardware implementation.

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